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10/613,904	07/03/2003	Satish R. Ganesan	X-949 US	7180

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,904	GANESAN ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/24/05 and,10/17/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) *42-45 and 49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41 and 46-48* is/are rejected.

7)☒ Claim(s) *41 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/613,904, and Amendment filed on 06/24/05. Applicants have elected claims 1-41, and 46-48 (Group 1) with traverse). Claims 42-45 and 49 (Group 2) are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/17/2005.

2. The possible invention of group I calculates arrival times by placing input variables of the function having later available times closer to the output location of function, thereby implementing delays/timing analysis and optimization; group II estimates product terms for the function using decomposing the function into a function tree consisting of AND, OR, NOT nodes and computing the array based on a function performed by the nodes, thereby performing functional analysis and functional optimization, not delays/timing analysis and optimization. Because these inventions are distinct for the reasons given above and the search required for Group 1 is not required for Group 2, restriction for examination purposes as indicated is proper. As such, the restriction is hereby made final.

3. In Amendment filed on 06/24/05 Applicant has included additional limitations into independent claims 1, 22, 24, 25, 47 and 48. The Examiner finds Applicant's comments persuasive on the application of Kaviani on the claims. However, the Examiner has found another reference, which in view of Kaviani reads on the claims as presently written.

Claim Objections

4. Change status of claims 42-45 and 49 from "(Original)" to – (Withdrawn)-- as recited in page 1 of the Applicant's "Response to restriction" filed 10/17/05.

5. Claims 25, 41, 46 and 48 are objected to because of following informalities:

In claims 25, 41, 46 and 48 after first appearance of the recitation of "softPALs" insert --, wherein softPAL is a complex function that when written in a sum-of-products (SOP) form is too wide to be implemented in a single LUT but can be implemented using a combination of these LUTS and dedicated logic elements --.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-35 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable by Kaviani et al. (US Publication No.: 20020079921 A1) in view of Lu et al. (US Patent 6,546,539).

7. As to claims 1, 22, 24, 25 and 48 Kaviani discloses:

(1) A method for mapping a function to logic in a programmable logic device having at least one look up table (LUT) and at least one dedicated logic element, the method comprising (Abstract; [0010]):

factoring (decompositioning) the function (logic) to derive a factored form of the function ([0017]; [0053]); and

implementing the factored form of the function using the dedicated logic element ([0017];[0054]);

(22) A programmable logic device configured to implement a function in factored form having a plurality of factored cube sets, wherein each factored cube set comprises a shared set and an unshared set, the programmable logic device comprising:

a first LUT (LUT 325, Fig.3B) configured to implement a first portion of the shared set of a first factored cube set ([0078]);

a second LUT (LUT 330, Fig.3B) coupled to implement a portion of the unshared set of the first factored cube set ([0078]); and

a first dedicated logic element (carry circuit 326, Fig.3B) coupling the first LUT and the second LUT to form a first LUT chain ([0078]);

(24) A programmable logic device, configured to implement a function in factored form having a plurality of factored cube sets, wherein each factored cube set comprises a shared set and an unshared set, the programmable logic device comprising:

a first combination of LUTS configured to implement a first factored cube set ([0095]);

a second combination of LUTS configured to implement a second factored cube set ([0097]); and

a first dedicated logic element coupling the first LUT and the second LUT to form a first LUT chain ([0099]-[0100]);

(25) A method of mapping a softPAL into a PLD comprising:

expressing the softPAL as a sum-of-products (SOP) function ([0054]- [0063]);

factoring the SOP function into at least one chain of factored cube sets (FCSs) having the form F(i) = <shared set> * <unshared set>,
where the shared set is a logical AND function of any number of variables, and the unshared set is a logical OR function of K or fewer logically ANDed variables, where K is a number of inputs to a lookup table (LUT) in the PLD ([0064]; [0078];[0085]- [0086]); and

implementing the at least one chain of FCSS with a combination of LUTS and dedicated resources ([0054]; [0078]);

(48) A method of mapping a function to a combination of one or more LUTS and softPALs, the method comprising:

forming factored cube sets (FCSS) from the function ([0054]; [0064]; [0078];[0085]- [0086]);

configuring a set of one or more vertical elements to perform a logical function ([0121]);

mapping the FCSs to a series of one or more LUTS performing logical functions ([0010]); and

coupling the one or more LUTS with the one or more vertical elements ([0122]-[0123]).

With respect to 1, 22, 24, 25 and 48 Kaviani teaches the features above but lacks a method for mapping a function to logic in a programmable logic device further comprising placing input variables of the function having later arrival times closer to the output location of the function than input variables having earlier arrival times.

8. As to claim 1, 22, 24, 25 and 48 Lu in view of Kaviani teaches:

A method for mapping a function to logic in an integrated circuit further comprising:

placing input variables of the function having later arrival times closer to the output location of the function than input variables having earlier arrival times (... mapping process includes the simple use of a Shannon expansion theorem equation to co-factor a Boolean function. The Shannon expansion theorem equation is used to move an input with a late arrival closer to the output of the Boolean function – col.1, ll.36-40) (col.5, ll.41-62).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Lu's teaching regarding the method for mapping a function to logic in the integrated circuit further comprising placing input variables of the function having later arrival times closer to the output location of the function than input variables having earlier arrival times and use it Kaviani's invention to optimize the netlist and physical placement for the programmable logic device that may satisfy the delay

requirements, using Shannon theorem calculations made in the technology mapping program, thereby improving a precision of the programmable logic device design.

9. As to claims 2-21, 23 26-35 and 48 Kaviani in view of Lu recites:

(2) The method of Claim 1, wherein implementing the factored form of the function using the dedicated logic element comprises: implementing a first and second portion of the factored form of the function using the LUT and the dedicated logic element ([0017];[0054]);

(3), (9), (17), (29), (31) The method, wherein factoring the function to derive a factored form of the function comprises forming a plurality of factored cube sets for the function ([0075]-[0078]);

(4), (5) The method, wherein the function comprises a plurality of p-terms, and forming a plurality of factored cube sets comprises:

forming a first factored cube set to accommodate a first p-term and

forming a second factored cube set to accommodate a second p-term when the first factored cube set cannot accommodate the second p-term ([0071]; [0075]; [0091]);

(6), (32) The method, wherein implementing the factored form of the function using a dedicated logic element, comprises: using a first LUT to perform a first function on a first portion of the shared set of a first factored cube set; using a second LUT to perform a second function on a portion of the unshared set of the first factored cube set; and forming a first LUT chain by coupling the first LUT and the second LUT using a first dedicated logic element of the programmable logic device ([0078]);

(7), (8), (13), (20), (23) The method, further comprising: using a third LUT to perform a third function on a second portion of the shared set of the first factored cube set and expanding the first LUT chain by coupling the third LUT to the first LUT chain using a second dedicated logic element of the programmable logic device ([0018]; [0075]-[0078]; [0122]-[0123]; [0144]);

(10), (33), (35) The method of Claim further comprising sorting variables of the shared set based on arrival time ([0053]; [0068]; [0102]);

(11) The method, maximum variable arrival time further comprising calculating a for each LUT ([0069]);

(12), (15), (21), (34) The method, wherein the first LUT chain is arranged based on the maximum variable arrival time of each LUT ([0094]; [0149]);

(14), (30) The method of Claim 13, wherein the second dedicated logic element is a cascade element that implements the OR function ([0120]);

(16) The method of Claim wherein implementing the factored form of the function using a dedicated logic element, comprises:

using a first combination of LUTS to implement a first factored cube set ([0095]-[0096]);

using a second combination of LUTS to implement a second factored cube set ([0097]-[0098]); and

forming a first LUT chain by coupling the first combination of LUTS and the second combination of LUTS using a first dedicated logic element of the programmable logic device ([0099]-[0100]);

(18), (19) The method, wherein the carry element is a multiplexer configured to implement a logical OR, AND function ([0099]; [0108]-[0109]);

(26) The method of Claim 25 further comprising: adding product terms to the unshared set to be implemented by a LUT until K is reached, then forming another FCS if additional product terms remain ([0078]);

(27) The method, wherein the combination of LUTS and dedicated resources is selected from several possible combinations to minimize delay of the overall function F ([0053]);

(28) The method of Claim 25 wherein three schemes are considered for the chain of FCSS with resources ([0055]).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 36-40 and 47 are rejected under 35 U.S.C. 102(e) as being unpatentable by Lu et al. (US Patent 6,546,539).

10. As to claims 36 and 47 Lu discloses:

(36) A method for mapping a function to logic elements a programmable logic device comprising:

factoring the function to derive a factored form of the function (col.5, ll.32-40; col.6, ll.62-66; col.7, ll.3-7);

determining arrival time (delay) for input signals to each factor in the factored form (Because all F's input gates and output gates are in the sub-netlist, the arrival time of each F's input can be calculated- col.7, ll.21-23) (col.7, ll.21-33); and

implementing the factored form of the function such that each factor is implemented by one of the logic elements (gates- Figs. 3 and 4), and factors having signals with the latest arrival times are implemented by logic elements closest to an output location of the function (col.1, ll.36-40; col.5, ll.41-62);

(47) A method for decreasing delay of a node in a critical path during a mapping of a function, comprising:

obtaining a first delay for the node based on a first element in a cost table (col.5, ll.36-40);

assigning the first delay to a delay of the node (col.5, ll.41-45);

selecting a second element in the cost table comprising a different number or inputs than the first element in the cost table (col.5, ll.45-58);

obtaining a second delay for the node based on a second element in the cost table (col.5, ll.58-62); and

assigning the second delay to the delay of the node when the second delay is smaller than the first delay (col.5, ll.31-32).

11. As to claims 37-40 Lu discloses:

(37), (39) The method, wherein a determination of which logic elements are closest to an output location is determined by using a cost table specifying delay for each softPAL that implements a factor (col.5, ll.32-63);

(38) The method, wherein the cost table includes softPAL listed in order of increasing delay (col.5, ll.52-56);

(40) The method, wherein each softPAL is selected from the plurality of possible softPALs based on minimizing delay (col.5, ll.31-32).

Allowable Subject Matter

12. Claims 41 and 46 are objected to, but would be allowable if rewritten in form including details of softPALs as recited above in the claims objection paragraph.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

(41) A post-mapping optimizing method comprising: (a) forming a mapped design mapped to a combination of look up tables (LUTS) and original sized softPALs, wherein softPAL is a complex function that when written in a sum-of-products (SOP) form is too wide to be implemented in a single LUT but can be implemented using a combination of these LUTS and dedicated logic elements; (b) calculating original critical path delay in the mapped design; (c) for each critical path in the mapped design re-mapping the critical path node to a larger sized softPAL, if delay is reduced, accepting the large sized softPAL, if delay is not reduced, retaining the LUT or original sized softPAL; (d) re-calculating a new critical path delay for a new mapped design; (e) if the new critical path

delay for the mapped design is less than the original critical path delay, accepting the new mapped design; and (f) repeating steps (a) through (e) until the new critical path delay for the mapped design is not less than the original critical path delay ([0091]);

(46) A method for determining a delay of a node for implementing a softPAL function using a combination of look up tables (LUTS) and dedicated logic elements, wherein softPAL is a complex function that when written in a sum-of-products (SOP) form is too wide to be implemented in a single LUT but can be implemented using a combination of these LUTS and dedicated logic elements, the method comprising: forming a first set of one or more FCS chains representing the equation; implementing the first set of FCS chains with a first implementation scheme; assigning the node a delay of the first implementation scheme; forming a second set of one or more FCS chains representing the equation; implementing the second set of FCS chains with a second implementation scheme; and updating the delay of the node when a delay of the second implementation scheme is less than the delay of the node.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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VUTHE SIEK
PRIMARY EXAMINER